REMARKS

Claims 1-6 and 8-18 are pending in this application. By this Amendment, claims 13-18 are added. The added claims introduce no new matter. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

The Office Action rejects claims 1-4, 6 and 8-12 under 35 U.S.C. §103(a) over Chen in view of U.S. Patent No. 7,087,963 to Suzuki; and rejects claim 5 under 35 U.S.C. §103(a) over Chen in view of Suzuki and further in view of U.S. Patent No. 5,576,230 to Guldi. These rejections are respectfully traversed.

The Office Action alleges that Chen discloses all of the features of the independent claims with the exception of (1) the taper angle of the gate electrode; (2) the second insulating film having a thickness of more than twice the thickness of the gate electrodes; and (3) the gate-insulating film being composed of silicon oxide. The Office Action alleges that the first two features would have been obvious optimizations, and relies on Suzuki as disclosing the composition of the gate-insulating film. The analysis of the Office Action fails for at least the following reasons.

As argued in the July 10, 2007 Request for Reconsideration, the Office Action has not established that the features of the second insulating layer having a thickness of more than twice the thickness of the gate electrode, and tapering the gate electrode between 20° and 80°, would have been obvious as mere optimization. The Office Action fails to establish that these features are result-effective variables, a necessary precondition for a finding of optimization. Additionally, Applicant has adequately disclosed unanticipated benefits of the claimed features.

In the December 27, 2006 Amendment, independent claims 1, 4, 5 and 10 were amended to include the feature of the second insulating layer having a thickness of more than twice the thickness of the gate electrode. The Office Action concedes that the applied

references do not disclose such a feature. However, the Office Action asserts that these features are *prima facie* obvious without a showing that the claimed ranges achieve unexpected results relative to the prior art range. The Office Action goes on to assert that there exists no evidence of record that the relative thicknesses provide unexpected results in the semiconductor device produced. These assertions are plainly incorrect.

On page 9 of the December 27, 2006 Amendment, Applicant stated that such relative thickness of the second insulating layer provides for a relatively long lightly doped drain (LDD), as described, for example, in paragraph [0078] of Applicant's specification. Applicant again directed the Examiner to this information on page 4 of Applicant's July 10, 2007 Request for Reconsideration. Clearly this is an unexpected result not obvious from the prior art.

In order to assert that any alleged optimization of any parameter would have been obvious, the Office Action is required to first establish by specific objective evidence that the claimed feature is regarded as a result-effective variable in the prior art (see MPEP §2144.05(II)(B)). In other words, the Office Action must provide support for why one of ordinary skill in the art would have been motivated to optimize the specific variable in question. Applicant maintains that no such objective evidence of record has been provided that can reasonably be considered to meet the above standard in showing even a suggestion that a relative thickness of a second insulating layer with respect to the gate electrode was a recognized result-effective variable for controlling LDD length with regard to configurations of the specific devices disclosed in the applied references.

Additionally, even if such a showing were made, the Examiner must still address Applicant's evidence that the relative thickness provides unexpected results in the semiconductor device produced (see MPEP §2144.05(III)).

This analysis applies equally to the ongoing failure to acknowledge and consider evidence repeatedly presented regarding the feature of tapering the gate electrode between 20° and 80° as well. Applicant has identified specific portions of the specification that disclose unanticipated benefits produced by these angles in Applicant's August 25, 2006 Amendment and July 10, 2007 Request for Reconsideration. Specifically, the attention of the Office Action is directed to paragraphs [0019] and [0082], and Fig. 11 of Applicant's disclosure. The Office Action simply repeats the assertion that this also considered as only optimization. This assertion is made without first establishing that the taper angle was recognized as a result-effective variable, with a showing of some specific objective evidence, in the prior art. The discounting of positively recited claim features, and inadequate rebuttal of Applicant's arguments, in an effort to render obvious the claims as *prima facie* obvious without any evidentiary support is improper.

Also, it is unclear which variable the Office Action indicates as being optimized among optimizing the taper angle to provide for device performance and then further optimizing the thickness of the second insulating layer relative to the gate electrode to provide for processing limitations and device performance. The applied references do not teach any corresponding method that would take into account both of these factors to achieve any disclosed improvement or even changes in device performance. The assertion that optimizing these two distinct variables to achieve an unspecified notional "optimal performance" is without basis.

Additionally, the Office Action relies on Suzuki as allegedly disclosing the claimed gate-insulating film being composed of silicon oxide. The Office Action refers to gate insulating film 13 of Suzuki as disclosing this feature. However, claim 1 recites, among other features, forming a gate-insulating film on the semiconductor film, the gate-insulating film being composed of silicon oxide, and forming a tapered gate electrode on the gate-insulating

film. Suzuki discloses two films, 13 and 14, both in Fig. 1 (Related Art) and the exemplary embodiment Fig. 4e. In both instances, the gate electrode 15 is formed on a second gate-insulating film 14 of SiN, not SiO_2. Accordingly, Suzuki does not teach the specific feature relied upon in the Office Action.

Further, the Suzuki method, and compositions of the Suzuki structure, would not have logically commended themselves to one of ordinary skill in the art looking to modify Chen based on the differences between Suzuki and Chen. Specifically, barrier layer 42 and insulating layer 40 in Chen are etched away prior to heavy ion implantation, as depicted in Fig. 2f. This is significantly different from the process described in Suzuki, in which the allegedly corresponding insulating layers 19 and 20 are applied completely over the gate electrode and surface of substrate 10 after forming the lightly doped drain ("LDD") and removal of resist 17. Thus, as with the previously-applied Kato reference, the protective films 19 and 20 in Suzuki cover the gate electrode and the allegedly corresponding gate-insulating film. Whereas, in Chen, the insulating layer 40 is etched away leaving only insulating spacer 46 that, as depicted in Fig,. 2e, does not cover either the gate electrode or the insulating layer 34. As such, no identified intended benefit of the specific compositions in Suzuki would have motivated one of ordinary skill in the art to modify the Chen method or apparatus in the manner suggested.

For at least the above reasons, the applied references are not combinable in the manner suggested, and no permissible combination of the applied references can reasonably be considered to have suggested the combinations of all of the features positively recited in claims 1, 4, 5 and 10. Additionally, claims 2, 3, 6, 8, 9, 11 and 12 would also not have been reasonably suggested by the applied references for at least the respective dependence of these claims, directly or indirectly, on an allowable base claim, as well as for the separately patentable subject matter that each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejection of claims 1-6 and 8-12 are respectfully requested.

Added claims 13-18 are also allowable for reasons similar to those discussed above, in addition to the separately patentable subject matter that each of these claims recites.

For example, claim 13 recites, among other features forming a layered insulating film composed of at least two different insulating films on the gate electrode on the substrate, the first insulating film having different composition from the gate-insulating film and the second insulating film having different composition from the first insulating film and thickness of more than twice a thickness of the gate electrode; etching an entire surface of the layered insulating film to form a predetermined pattern by dry etching process, the predetermined pattern having a width greater than a width of the gate electrode and smaller than a width of the semiconductor film. The applied references cannot reasonably be considered to have suggested such features at least because Chen discloses the method of wet etching process to remove the insulating layer on the gate insulating layer. The claim amendments are supported by paragraphs [0084] and [0085] of Applicant's specification, as filed. Normally, dry etching process performs high accuracy etching compared with wet etching process. Also, it is not necessary to change the process from dry to wet. Thus, the present subject matter provides for achieving an accurate LDD with a simple process.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-6 and 8-18 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

James E. Golladay, II
Registration No. 58,182

JAO:JEG/clf

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OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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